REMARKS

In sections 3 and 4 of the Office Action, the Examiner rejected claims 3, 4, 7, 8, 11, 12, 15, and 16 under 35 U.S.C. §112, second paragraph, as failing to particularly point out and distinctly claim the invention. Specifically, the Examiner appears to assert that the specification does not describe the mesas as being silicon mesas and, therefore, references in these claims to the mesas being silicon mesas is not supported by the specification.

The Examiner's attention is directed to page 8, lines 9-13 of the specification which states that "[t]he SOI substrate 12 typically includes a silicon handle wafer, a buried oxide layer over the silicon handle wafer, and one or more silicon layers that are over the buried oxide layer and that are processed to form electronic devices of the integrated circuit." The silicon handle wafer is later described in specification and shown in the drawings (e.g., see Figure 5) as the layer 40, the buried insulating layer is later described in specification and shown in the drawings (e.g., see Figure 5) as the layer 42, and the one or more silicon layers is shown in the drawings as the layer 44. Also, the specification describes the layer 44 as an n^- layer,

a nomenclature frequently used in connection with silicon. Furthermore, the one or more silicon layers are described as the layers in which devices are formed and the mesas are described as device mesa. Accordingly, it is clearly understood from the specification and drawings that the device mesas can be silicon.

Therefore, claims 3, 4, 7, 8, 11, 12, 15, and 16 satisfy the requirements of 35 U.S.C. §112, second paragraph.

In sections 5 and 6 of the Office Action, the Examiner rejected claims 1, 2, 5, 6, 9, 10, 13, 14, and 17-19 under 35 U.S.C. §103(a) as being unpatentable over the Librizzi patent in view of the Hirabayashi patent.

The Librizzi patent discloses an integrated circuit 20 having a SOI substrate 22. The SOI substrate 22 includes two isolation trenches 24 and 26 that isolate a first device mesa 28 and two isolation trenches 30 and 32 that isolate a second device mesa 34. The isolation trenches 24 and 26 define a first guard ring region 36, and the isolation trenches 30 and 32 define a second guard ring region 38. The isolation trenches 24, 26, 30, and 32 may be filled with silicon oxide or oxide/polysilicon.

The SOI substrate 22 includes a silicon support substrate 40 and an insulating layer 42. The insulating layer 42 may be a silicon oxide film. The silicon support substrate 40 is preferably formed of a high resistivity (or high "Z") substrate having a high Ohm-centimeter rating, such as, for example, a 1 KΩ-centimeter substrate.

An n-type buried layer 46 extends into the first guard ring region 36, and an n-type collector 48 is implanted into the first guard ring region 36. The n-type collector 48 is heavily doped. Metal contacts 50 are made to the n-type collector 48 of the first guard ring region 36 to provide a low resistance RF ground along conductors 52. The second guard ring region 38 is similarly constructed.

The first and second guard ring regions 36 and 38 provide RF isolation. The insulating layer 42 provides additional RF isolation. The use of a high Z substrate 40 improves RF isolation by making the substrate 40 a high resistance path for RF power.

As can be seen and as the Examiner recognizes, the Librizzi patent does not disclose or suggest a guard ring that is in contact with the semiconductor substrate

as recited in independent claims 1, 20 and 39. Therefore, the Examiner relies on the Hirabayashi patent.

The Hirabayashi patent discloses an integrated circuit having a digital circuit 2 and an analog circuit 4 both fabricated on a common silicon substrate 6. A cross-talk source isolator 8 is provided in the substrate 6 so as to surround the digital circuit 2.

Figure 2 shows an arrangement having a substrate contact region 10 and a metal line 12 coupled to ground. The region 10 contains the same conductive type impurity as a substrate 20 and is electrically conductive. The substrate 20 contains impurity and thus exhibits a low electrical resistance. A silicon well 22 is grown on the substrate 20 and is processed to form drains and sources of electronic devices. A layer 24 is provided as an element segregation layer. The electronic devices also have MOS gate oxides 28, MOS polycrystalline silicon gates 28, a lightly-doped drain region 30, source and drain regions 32, and MOS gate side walls 34. Insulating layers 35 and 36 and source and drain electrodes 50 are also provided.

Cross-talk reduction relies on the substrate contact 10 and the metal line 12. According to the Hirabayashi patent, noise 11a in the silicon well 22 is

conducted to ground through the diffused region 10, but noise 11b in the low resistance substrate 20 is transferred between circuits by way of the substrate 20.

Instead of using the substrate contact 10 and the metal line 12 for isolation, Figure 3 shows the use of a trench 14 containing a dielectric 16. The dielectric 16 also is unable to prevent cross-talk being transferred through the substrate 20.

Figures 4-8 show an embodiment in which a trench 38 surrounding one of the digital and analog circuits is filled with an oxide 42 and a doped polycrystalline silicon or tungsten 44 that electrically connects the low resistance substrate 20 to ground though a contact 50e. The conductor 44 guides cross-talk in the substrate 20 to ground.

The Examiner asserts that it would have been obvious in view of the Hirabayashi patent to extend the guard rings 36 and 38 disclosed in the Librizzi patent to the silicon support substrate 40 because such extensions would aid in preventing cross talk.

However, the Examiner has not shown that extending the guard rings 36 and 38 disclosed in the Librizzi patent to the silicon support substrate 40 would aid in preventing cross talk. Indeed, the combination of

the Librizzi patent and the Hirabayashi patent suggest no such thing to one of ordinary skill in the art.

The problem as postulated by the Librizzi patent and the Hirabayashi patent is to prevent noise from migrating through the substrate from one electronic device to another. The solution offered by the Hirabayashi patent is to ground the substrate, which works according to the Hirabayashi patent in the case where the substrate is a low resistivity substrate and is, therefore, conductive. On the other hand, the solution offered by the Librizzi patent is to replace the low resistivity substrate for a high resistivity substrate and to add an insulator over the low resistivity substrate for good measure. The Librizzi patent states that a high resistivity substrate provides a high resistance path for RF power. One of ordinary skill in the art would understand that such a high resistivity substrate is a poor conductor that would not conduct noise through it.

Accordingly, taken together, these patents suggest that the grounding of the substrate is needed if the substrate is conductive and is not needed if the substrate is a non-conductive high resistivity substrate. Therefore, since the substrate 40 as disclosed in the

Librizzi patent is a non-conductive high resistivity substrate, extending the guard ring 36 of the Librizzi patent to the substrate 40 would not occur to one of ordinary skill in the art.

The Examiner points to column 2, lines 45-50 (presumably of the Hirabayashi patent) to support the assertion that extending the guard rings 36 and 38 disclosed in the Librizzi patent to the silicon support substrate 40 would aid in preventing cross talk. This passage states that it is an object of the Hirabayashi patent to provide an isolator for minimizing cross talk through a substrate. However, the context of this passage in the Hirabayashi patent is that such cross-talk is only a problem if the substrate is a low resistivity substrate and, therefore, conductive to such cross talk. When the substrate is a high resistivity substrate such as disclosed in the Librizzi patent, the Hirabayashi patent implicitly suggests that this passage is not pertinent.

Therefore, contrary to the assertion of the Examiner, it would not have been obvious to one of ordinary skill in the art to combine the Librizzi patent and the Hirabayashi patent in a manner that would meet the limitations of independent claims 1, 20 and 39.

Accordingly, independent claims 1, 20, and 39 are not unpatentable over the Librizzi patent in view of the Hirabayashi patent.

Because independent claims 1, 20, and 39 are not unpatentable over the Librizzi patent in view of the Hirabayashi patent, dependent claims 2-19 and 21-31 are likewise not unpatentable over the Librizzi patent in view of the Hirabayashi patent.

In section 7 of the Office Action, the Examiner rejected claims 3, 4, 7, 8, 11, 12, 15, and 16 under 35 U.S.C. §103(a) as being unpatentable over the Librizzi patent in view of the Hirabayashi patent and further in view of the Beyer patent.

However, the Beyer patent does not disclose guard rings of any variety and, therefore, does not cure then deficiencies of the Librizzi patent and the Hirabayashi patent.

Accordingly, independent claims 1, 20, and 39 are not unpatentable over the Librizzi patent in view of the Hirabayashi patent and further in view of the Beyer patent. Because independent claims 1, 20, and 39 are not unpatentable over the Librizzi patent in view of the Hirabayashi patent and further in view of the Beyer patent, dependent claims 3, 4, 7, 8, 11, 12, 15, and 16

are likewise not unpatentable over the Librizzi patent in view of the Hirabayashi patent and further in view of the Beyer patent.

CONCLUSION

In view of the above, it is clear that the claims of the present application are patentable over the art applied by the Examiner. Accordingly, allowance of these claims and issuance of the above captioned patent application are respectfully requested.

Respectfully submitted,

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